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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/618,225	07/11/2003	Daniel John McNamara	G00631.70037 sjh	4403

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EXAMINER	
CAI, WAYNE HUU	
ART UNIT	**PAPER NUMBER**
2617	

SHORTENED STATUTORY PERIOD OF RESPONSE	MAIL DATE	DELIVERY MODE
3 MONTHS	03/19/2007	PAPER

Please find below and/or attached an Office communication concerning this application or proceeding.

If NO period for reply is specified above, the maximum statutory period will apply and will expire 6 MONTHS from the mailing date of this communication.

Office Action Summary	Application No.	Applicant(s)	
	10/618,225	MCNAMARA ET AL.	
	Examiner	Art Unit	
	Wayne Cai	2617	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *11 July 2003*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-41* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-19,21-23 and 26-41* is/are rejected.

7)☒ Claim(s) *20,24 and 25* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *10 May 2004* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

Information Disclosure Statement

The information disclosure statement (IDS) submitted on March 15, 2004 is being considered by the examiner.

Drawings

The drawings were received on May 10, 2004. These drawings are acceptable.

Claim Objections

Claim 15 is objected to because of the following informalities:

The dependency of claim 15 is incorrect. Appropriate correction is required.

Claim Rejections - 35 USC § 102

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

Claims 1-19, 22, 23, and 26-41are rejected under 35 U.S.C. 102(b) as being anticipated by Bell et al. (hereinafter "Bell", US 6,038,400. Note: Applicant cited reference).

Regarding claims 1, 36, and 37, Bell teaches or suggests a method for communicating through an interface circuit between a device associated with the interface circuit and an external device in either one of a first communication protocol and a second communication protocol, the method comprising the steps of (see title, and abstract). Bell further teaches or suggests providing the interface circuit with a plurality of communication terminals for communicating with the external device (i.e., terminals 50, 30, 36, 34, and 48 of fig. 1 and its descriptions), the number of communicating terminals required not exceeding the number of communicating terminals required to communicate in the one of the first and second protocols which requires the greatest number of communication terminals (col. 11,line 28 – col. 12, line 8). Bell also discloses providing the interface circuit with a monitoring circuit for monitoring one of the communication terminals for a protocol select signal, monitoring the one of the communication terminals by the monitoring circuit for the protocol select signal, and configuring the interface circuit in a second protocol mode for communicating in the second protocol in response to detection of the protocol select signal (i.e., the protocol identifying circuitry 24 senses DIN line 34 and generates mode select signals 22 to configure protocol implementing circuitry 20 for the increment or decrement protocol. See col. 7, lines 4-31).

Bell also teaches or suggests following a reset signal the protocol implementing circuitry 20 is configured to use a predetermined protocol, and reset circuitry 14 is coupled to supply voltage so that a reset signal is generated following the initial application of power to integrated circuit 10 at col. 6, lines 4-26 reads on configuring the

interface circuit in a first protocol mode on power-up of the interface circuit for communicating in the first protocol.

Regarding claims 2, and 38, Bell discloses all limitations recited within claims as described above. Bell also discloses in which a locking circuit responsive to the monitoring circuit detecting the protocol select signal is provided for locking the interface circuit configured in the second protocol mode (abstract).

Regarding claim 3, and 39, Bell discloses all limitations recited within claims as described above. Bell also discloses in which the locking circuit is responsive to the monitoring circuit detecting the protocol select signal for locking the interface circuit configured in the first protocol mode (i.e., when the power of integrated circuit 10 is on until different protocol is detected).

Regarding claims 4, 5, 40, and 41, Bell discloses all limitations recited within claims as described above. Bell also teaches or suggests in which the locking circuit is responsive to powering down of the interface circuit for releasing the interface circuit from the configured protocol mode (i.e., following a reset signal the protocol implement circuitry 20 is configured to use a predetermined protocol).

Regarding claim 6, Bell discloses all limitations recited within claims as described above. Bell also discloses in which a signal processing circuit is provided, the signal processing circuit being selectively and alternately configurable in one of the first and second protocol modes for processing the communication signals in the respective first and second protocols, the signal processing circuit being configurable in

the respective first and second protocol modes in response to first and second mode select signals, respectively (col. 7, line 1 – col. 8, line 10).

Regarding claim 7, Bell discloses all limitations recited within claims as described above. Bell also discloses in which a switch circuit is provided, the switch circuit being selectively and alternately operable in one of a first state and a second state in response to the monitoring circuit, the switch circuit being operable in the first state in response to the monitoring circuit on power-up of the interface circuit for applying the first mode select signal to the signal processing circuit (col. 6, lines 15-26).

Regarding claims 8, 9, and 10, Bell discloses all limitations recited within claims as described above. Bell also discloses in which the switch circuit is operable in the second state in response to the monitoring circuit detecting the protocol select signal for applying the second mode or the first mode select signal to the signal processing circuit (col. 8, line 22 – col. 9, line 60, table 1 and its descriptions).

Regarding claim 11, Bell discloses all limitations recited within claims as described above. Bell also discloses in which the first mode select signal is one of a logic high and a logic low signal, and the second mode select signal is the other of a logic high or a logic low signal (col. 8, lines 22-67, and table 1 and its descriptions).

Regarding claim 12, Bell discloses all limitations recited within claims as described above. Bell also discloses in which the logic high signal which provides the one of the first and second mode select signals is provided by the supply voltage of the interface circuit, and is applied to the signal processing circuit through the switch circuit when the switch circuit is in the first state (col. 6, lines 15-26).

Regarding claim 13, Bell discloses all limitations recited within claims as described above. Bell also discloses in which the logic low signal which provides the one of the first and second mode select signals is provided by ground of the interface circuit, and is applied to the signal processing circuit through the switch circuit when the switch circuit is in the second state (col. 6, lines 15-26).

Regarding claim 14, Bell discloses all limitations recited within claims as described above. Bell also discloses in which one of the communication terminals is adapted for selectively receiving one of the first and second mode select signals simultaneously with the protocol select signal being applied to another one of the communication terminals (col. 5, line 61 – col. 6, line 3), and a mode signal latching means is provided responsive to the protocol select signal for latching the one of the first and second mode select signals applied to the communication terminal (col. 8, lines 22-41).

Regarding claim 15 Bell discloses all limitations recited within claims as described above. Bell also discloses in which the latched one of the first and second mode select signals is applied from the mode signal latching means to the signal processing circuit through the switch circuit, when the switch circuit is in the second state (col. 10, line 28 – col. 11, line 27).

Regarding claim 16, Bell discloses all limitations recited within claims as described above. Bell also discloses in which the switch circuit comprises a multiplexer (col. 8, lines 22-41).

Regarding claim 17, Bell discloses all limitations recited within claims as described above. Bell also discloses in which the monitoring circuit comprises a first state machine for monitoring the communication terminal on which the protocol select signal is to be applied, and for outputting one of a logic high and a logic low signals in response to the interface circuit being powered up, and the other of the logic high and the logic low signals on the protocol select signal being detected, the switch signal outputted by the monitoring circuit being derived from the logic signal outputted by the first state machine (col. 6, lines 15-67).

Regarding claim 18, Bell discloses all limitations recited within claims as described above. Bell also discloses in which a switch signal latching means is provided for alternately latching the switch signal in the one of the high and low logic states in response to the logic state of the output signal of the first state machine (col. 15, lines 35-50).

Regarding claim 19, Bell discloses all limitations recited within claims as described above. Bell also discloses in which the switch signal latching means is responsive to the protocol select signal after power-up of the interface circuit for altering the logic state of the switch signal for operating the switch circuit from the first state to the second state, and for latching the switch signal in the altered logic state (col. 15, lines 35-50).

Regarding claim 22, Bell discloses all limitations recited within claims as described above. Bell also discloses in which the protocol select signal comprises a

signal which transitions from one of high and low states to the other of the high and low states (col. 10, lines 28-38).

Regarding claim 23, Bell discloses all limitations recited within claims as described above. It is inherent that the monitoring circuit is responsive to one of a rising and falling edge of the protocol select signal as the protocol select signal transitions from the one of the high and low states to the other of the high and low states because high and low state corresponds to high and low voltage (i.e., the logic value of either "0" and "1" as known in the art.) Since Bell clearly teaches or suggests the monitoring circuit is responsive to one of the transition of the signal from high-to-low and/or from low-to-high; hence, the claimed feature is inherent.

Regarding claim 26, Bell discloses all limitations recited within claims as described above. Bell also discloses in which one of the first and second protocols is SPI protocol, and the other of the first and second protocols is one or both of I^2C and SMBus protocols (col. 10, lines 28-33).

Regarding claim 27, Bell discloses all limitations recited within claims as described above. Bell also discloses in which at least three communication terminals are provided for facilitating communication in both the SPI protocol and one or both of the I^2C and SMBus protocols (see table 2).

Regarding claim 28, Bell discloses all limitations recited within claims as described above. Bell also discloses in which one of the communication terminals is a clock signal receiving terminal for receiving clock signals for communicating in the SPI protocol and one or both of the I^2C and SMBus protocols, and one of the

communication terminals is a chip enable terminal for receiving a chip enable signal for communicating in the SPI protocol (see fig. 4 & fig. 5 and its descriptions).

Regarding claim 29, Bell discloses all limitations recited within claims as described above. Bell also discloses in which at least one of the communication terminals is a serial data address terminal for communicating serial data in the SPI protocol, and for communicating serial data and addresses in one or both of the I^2C and SMBus protocols (see fig. 5 and its descriptions).

Regarding claim 30, Bell discloses all limitations recited within claims as described above. Bell also discloses in which two of the communication terminals are serial data address terminals, one of which communicates serial data into the interface circuit, and one of which communicates serial data out of the interface circuit in the SPI protocol, and one of the two serial data address terminals communicates serial data and addresses with the interface circuit in one or both of the I^2C and SMBus protocols (col. 3, lines 22-36).

Regarding claim 31, Bell discloses all limitations recited within claims as described above. Bell also discloses in which terminal is provided for receiving clock signals for communicating in the I^2C and/or SMBus protocols, and one of the two serial data address terminals communicates addresses with the interface circuit in one or both of the I.sup.2C and SMBus protocols (col. 3, lines 22-36).

Regarding claim 32, Bell discloses all limitations recited within claims as described above. Bell also discloses in which the first protocol is one or both of the I^2C and SMBus protocols (col. 10, lines 28-33).

Regarding claim 33, Bell discloses all limitations recited within claims as described above. Bell also discloses in which the chip enable terminal is adapted for receiving the protocol select signal (col. 7, lines 48-66).

Regarding claim 34, Bell discloses all limitations recited within claims as described above. Bell also discloses in which one of the serial data address terminals is adapted for receiving the first and second mode select signals (col. 11, lines 1-15).

Regarding claim 35, Bell discloses all limitations recited within claims as described above. Bell also discloses an associated device, the interface circuit being provided for communicating the associated device with an external device in either of the first protocol and the second protocol (abstract).

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

Claim 21 is rejected under 35 U.S.C. 103(a) as being unpatentable over Bell et al. (hereinafter "Bell", US 6,038,400) in view of Freidin (US 4,967,346).

Regarding claim 21, Bell discloses all limitations recited within claims as describe above, but does not specifically disclose the features of claim 21.

In a similar endeavor, Freidin discloses a universal microprocessor interface circuit. Freidin also disclsoes in which a second state machine is provided, the second

state machine being responsive to the mode select signal applied to the signal processing circuit for applying a timing select signal to the signal processing circuit, for selecting the timing of the signal processing circuit to correspond with the one of the first and second protocol modes in which the signal processing circuit is configured (fig. 3 and its descriptions).

Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to combine Bell in view of Freidin.

The motivation/suggestion for doing so would have been to properly provide timing signals depend on the type of the protocols.

Allowable Subject Matter

Claims 20, 24, 25 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Wayne Cai whose telephone number is (571) 272-7798. The examiner can normally be reached on Monday - Thursday from 7:00-5:00.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Duc Nguyen can be reached on (571) 272-7503. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

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